

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:  
an internal circuit having first and second  
external terminals;

5 first and second fuse elements, each having first  
and second terminals, the first terminals of the first  
and second fuse elements being respectively connected  
to the first and second external terminals; and

a discharge line connected to the second terminals  
10 of the first and second fuse elements and serving as  
an electrostatic discharge current path.

2. The semiconductor integrated circuit according  
to claim 1, wherein:

the internal circuit further has a MOS transistor  
15 having a gate connected to the first external terminal;  
and

each of the first and second fuse elements has  
a resistance value that satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

20 where  $V_{OX}$  represents a breakdown voltage of a gate  
oxide film of the MOS transistor,  $R_m$  represents a wire  
resistance value in the electrostatic discharge current  
path between the first and second external terminals,  
 $R_x$  represents a resistance value of all fuse elements  
25 arranged in the electrostatic discharge current path  
between the first and second external terminals, and  
 $I_{esd}$  represents a value of an electrostatic discharge

current.

3. The semiconductor integrated circuit according to claim 1, wherein the fuse elements remain firm even when energy of  $200\mu\text{J}$  is applied thereto.

5           4. The semiconductor integrated circuit according to claim 1, wherein the fuse elements remain firm even when energy of  $200\mu\text{J}$  is applied thereto but break when a direct current of 30mA is applied thereto within 20 seconds.

10           5. The semiconductor integrated circuit according to claim 1, wherein the fuse elements are electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

15           6. A semiconductor integrated circuit comprising:  
an internal circuit having first and second external terminals;

an electrostatic protecting circuit connected to the second external terminal;

20           a fuse element having first and second terminals,  
the first terminal of the fuse element being connected to the first external terminal; and

25           a discharge line connected to the electrostatic protecting circuit and the second terminal of the fuse element and serving as an electrostatic discharge current path.

7. The semiconductor integrated circuit according to claim 6, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that  
5 satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where  $V_{OX}$  represents a breakdown voltage of a gate oxide film of the MOS transistor,  $R_m$  represents a wire resistance value in the electrostatic discharge current  
10 path between the first and second external terminals,  $R_x$  represents a resistance value of the fuse element, and  $I_{esd}$  represents a value of an electrostatic discharge current.

8. The semiconductor integrated circuit according  
15 to claim 6, wherein the fuse element remains firm even when energy of  $200\mu J$  is applied thereto.

9. The semiconductor integrated circuit according to claim 6, wherein the fuse element remains firm even when energy of  $200\mu J$  is applied thereto but breaks  
20 when a direct current of 30mA is applied thereto within 20 seconds.

10. The semiconductor integrated circuit according to claim 6, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit  
25 is mounted on a circuit board.

11. A semiconductor integrated circuit comprising:  
an internal circuit having first, second and third

external terminals;

a fuse element having first and second terminals,  
the first terminal of the fuse element being connected  
to the first external terminal;

5 first and second electrostatic protecting circuits  
respectively connected to the second and third external  
terminals;

a first discharge line connected to the first and  
second electrostatic protecting circuits and serving as  
10 an electrostatic discharge current path; and

a second discharge line connected to the second  
terminal of the fuse element and the second external  
terminal and provided to keep the first and second  
external terminals at substantially the same potential.

15 12. The semiconductor integrated circuit according  
to claim 11, wherein:

the internal circuit further has a MOS transistor  
having a gate connected to the first external terminal;  
and

20 the fuse element has a resistance value that  
satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where  $V_{OX}$  represents a breakdown voltage of a gate  
oxide film of the MOS transistor,  $R_m$  represents a wire  
25 resistance value in the electrostatic discharge current  
path between the first and second external terminals  
or between the first and third external terminals,  $R_x$

represents a resistance value of the fuse element, and  $I_{esd}$  represents a value of an electrostatic discharge current.

13. The semiconductor integrated circuit according  
5 to claim 11, wherein the fuse element remains firm even when energy of  $200\mu J$  is applied thereto.

14. The semiconductor integrated circuit according  
to claim 11, wherein the fuse element remains firm even  
when energy of  $200\mu J$  is applied thereto but breaks  
10 when a direct current of  $30mA$  is applied thereto within  
20 seconds.

15. The semiconductor integrated circuit according  
to claim 11, wherein the fuse element is electrically  
disconnected when the semiconductor integrated circuit  
15 is mounted on a circuit board.

16. A semiconductor integrated circuit comprising:  
a digital circuit having a first external  
terminal;

a first electrostatic protecting circuit connected  
20 to the first external terminal;

a first discharge line connected to the first  
electrostatic protecting circuit and serving as  
an electrostatic discharge current path;

an analog circuit having a second external  
25 terminal;

a second electrostatic protecting circuit  
connected to the second external circuit;

a second discharge line connected to the second electrostatic protecting circuit and serving as an electrostatic discharge current path; and

5 a fuse element connected between the first and second discharge lines and serving as an electrostatic discharge current path of the digital and analog circuits.

17. The semiconductor integrated circuit according to claim 16, wherein:

10 the digital circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

15 
$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where  $V_{OX}$  represents a breakdown voltage of a gate oxide film of the MOS transistor,  $R_m$  represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, 20  $R_x$  represents a resistance value of the fuse element, and  $I_{esd}$  represents a value of an electrostatic discharge current.

18. The semiconductor integrated circuit according to claim 16, wherein the fuse element remains firm even 25 when energy of  $200 \mu J$  is applied thereto.

19. The semiconductor integrated circuit according to claim 16, wherein the fuse element remains firm even

when energy of  $200\mu\text{J}$  is applied thereto but breaks  
when a direct current of  $30\text{mA}$  is applied thereto within  
20 seconds.

20. The semiconductor integrated circuit according  
5 to claim 16, wherein the fuse element is electrically  
disconnected when the semiconductor integrated circuit  
is mounted on a circuit board.